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Revision History

Version	Date	Description	Author
1.0.0	11/09/2021	Initial Create	maweishuo

Terms and Acronyms

Terms and Acronyms	Definition
CF	Compact Flash
SM	Smart Media
XD	xD picture
SD	Secure Digital
Micro SD	Micro Secure Digital
MS	Memory Stick
MS Pro	Memory Stick Pro
MMC	Multimedia Card
SDRAM	Synchronous Dynamic Random Access Memory
MD	MicroDrive
TF	T Flash
LCD	Liquid Crystal Display
ICE	In-circuit emulation, or in-circuit emulator
JTAG	Joint Test Action Group(ANSI/ICEEE Std.11149.1-1990)
PQFP	Plastic Quad Flat Package
LQFP	Low-Profile Quad Flat Package
BGA	Ball Grid Array
PIP	Picture In Picture
TAP	TEST ACCESS PORT
RGB	Red-Green-Blue color space representation
TCON	Timing controller

General Conventions

Symbol	Description

1 Introduction

1.1 Overview

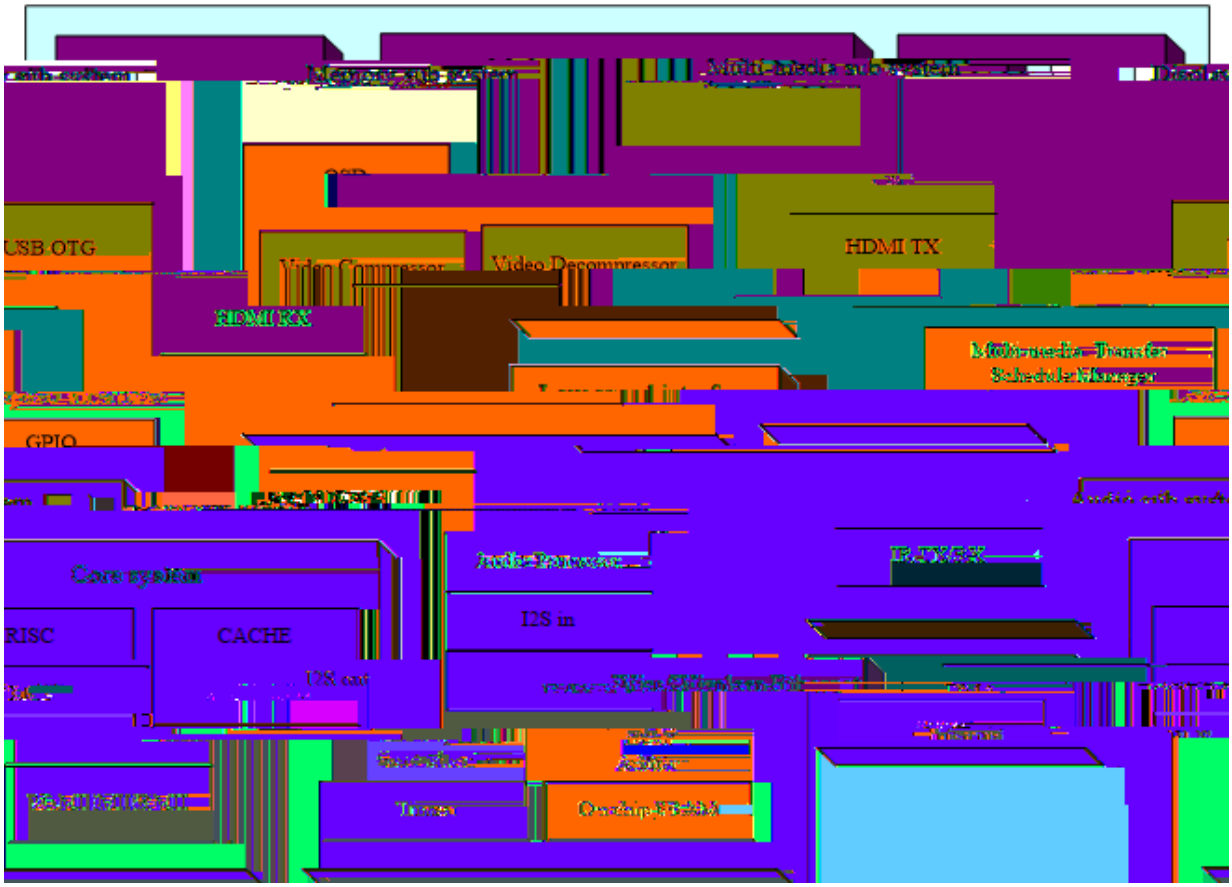
The AM8370 processor from Actions-Micro is a highly integrated mix signal SoC target at multi-media applications. The AM8370 emmedded CPU is a high performance, low power 32bit RISC core with DSP instruction extension, which can run as fast as 700MHz.

The AM8370 integrated lossless or near-lossless image/video compress and de-compress module which c3.480n transfer 1080P video with format H.264 through 1Gbit/s Ethernet.

The AM8370 multi-media processor provided display solutions with the help of on chip HDMI transmitter and receiver interface.

AM8370 is also integrated with 1 USB OTG controllers, UART, I2C, SPI, etc.

Block Diagram



AM8370 BLOCK DIAGRAM

3 Power on Sequence

The power on sequence requirements of the AM7xxx and AM8xxx products are the same, which are shown in the following figure. VDD represents the power pins supplying power for the core. VCC represents the power pins supplying power for the general purpose pads. SVCC represents the power pins supplying power for the DDR2 or DDR3 SDRAM related pads. P_RESETB is the asynchronous reset pin. PWROK is an internal signal. It is low during the power-on phase to reset all the registers in the chip. The system boots at the moment when PWROK turns to high.

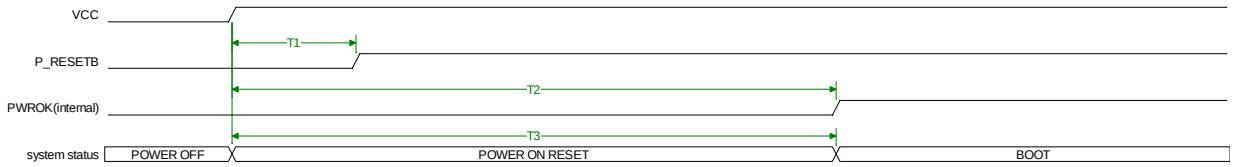


Figure 1 Power on Sequence Diagram

Timing Requirements:

1. $T1$ $20ms$
2. $T2$ $128ms$
3. $T3$ is equal to the greater one between $T1$ and $T2$
4. The power on sequence of VDD/VCC/SVCC is not cared

4 Pin Out Specification

Pin out table

PIN NUM	PIN NAME	TYPE	Function
1	P_SPINSS	B	SPI_NSS
2	VCC3	PWR	VCC3

36	P_UARTRX1	B	GPIO18
37	P_EXTINT0	B	EXTINT0
38	P_EXTINT1	B	GPIO32/I2STMCLK
39	P_I2SSCK	B	I2SSCK/IRRX
40	P_I2SSD	B	I2SSD/I2STSD
41	P_I2SWS	B	I2SWS/I2STWS
42	P_MACRVLD	B	RGMII_RXCTL
43	P_MACMDIO	B	MACMDIO
44	P_MACMDC	B	MACMDC
45	P_MACTVLD	B	RGMII_TXCTL
46	P_MACTD1	B	RGMII_TXD0
47	P_MACTD0	B	RGMII_TXD1
48	P_MACTCLK	B	RGMII_TXCLK
49	VCC0(2.5V)	PWR	VCC0(2.5V)
50	P_MACRD1	B	RGMII_RXD1
51	P_MACRD0	B	RGMII_RXD0
52	P_MACTD2	B	RGMII_TXD2
53	P_MACTD3	B	RGMII_TXD3
54	P_MACRD2	B	RGMII_RXD2
55	P_MACRD3	B	RGMII_RXD3
56	P_MACTER	B	MAC_CLKO
57	P_MACRCLK		

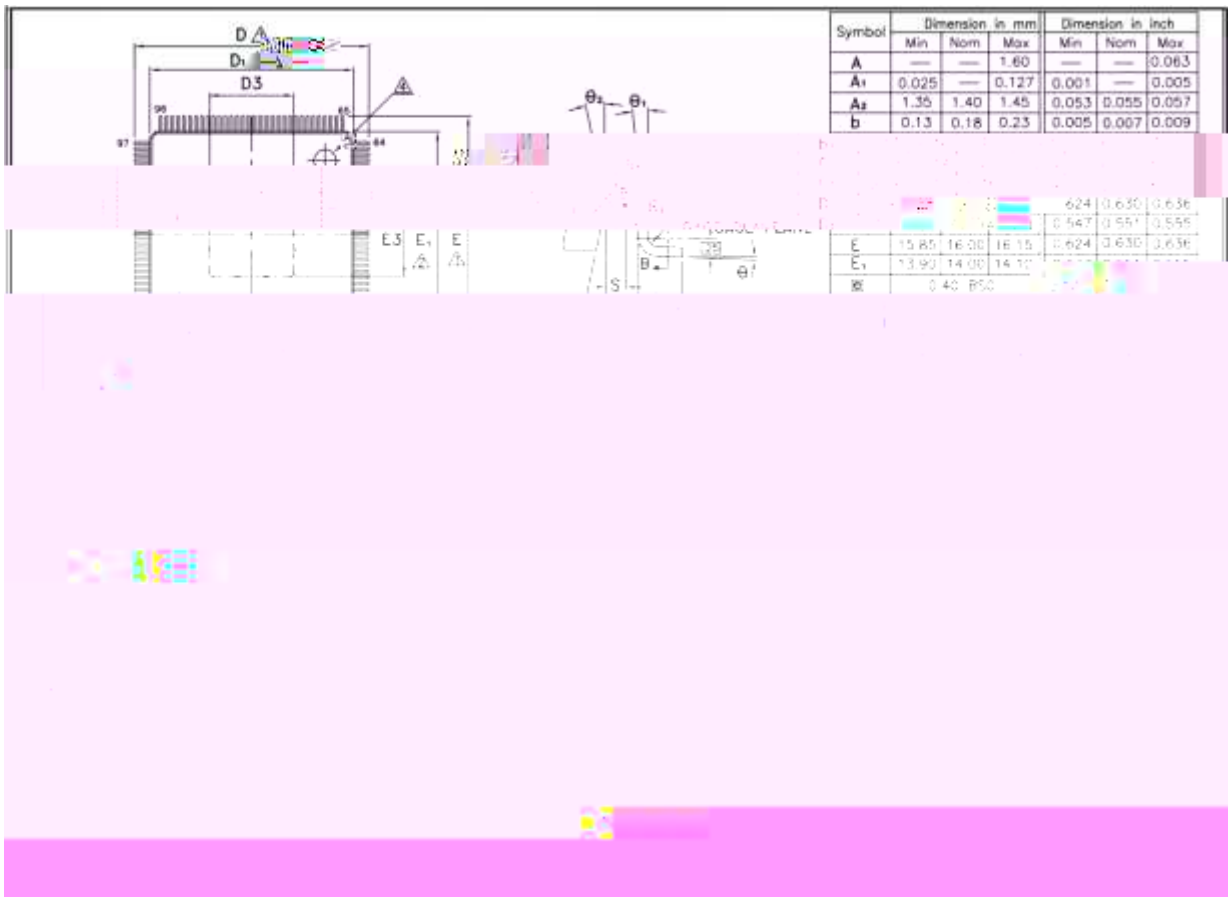
79	P_DDRBA1	B	P_DDRBA1
80	P_DDRBA0	B	P_DDRBA0
81	P_DDRBA2	B	P_DDRBA2
82	P_DDRWEB	B	P_DDRWEB
83	VDD	PWR	VDD
84	SVCC	PWR	SVCC
85	P_DDRDQ4	B	P_DDRDQ4
86	P_DDRDQ3	B	P_DDRDQ3
87	P_DDRDQ1	B	P_DDRDQ1
88	P_DDRDQ6	B	P_DDRDQ6
89	P_DDRDQ12	B	P_DDRDQ12
90	P_DDRDQ11	B	P_DDRDQ11
91	P_DDRDQ9	B	P_DDRDQ9
92	P_DDRDQ14	B	P_DDRDQ14
93	P_DDRDM1	B	P_DDRDM1
94		B	P_DDRDM0

6 Crystal Requirements

Requirements for 24MHz oscillator.

Description	Specification Requirement

7 Mechanical Specification



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.025	—	0.127	0.001	—	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10			
e		0.40 BSC				